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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIRST SEMESTER M.TECH DEGREE EXAMINATION, APR 2021/DEC 2021

Branch:ELECTRONICS AND COMMUNICATION

Stream: VLSI AND EMBEDDED SYSTEMS

Course Code & Name: 01EC6613 ELECTRONIC DESIGN AUTOMATION TOOLS

Answer *any two full* questions from *each* part

Limit answers to the required points.

Max. Marks: 60 Duration: 3 hours

PART A

1. a. Discuss with diagrams the design methodology for Integrated circuits with reference to the Y chart? 4.5 marks

   b. What is the purpose of optimization in different stages of digital design? Explain your answer by giving the steps from VHDL description to netlist and the strategies followed for optimization? 4.5 marks

2. a. Explain the differences between Top Down and Bottom up approach for chip design? Which of these is advantageous for digital design? 4.5 marks

   b. Discuss the retiming algorithms in the synthesis of synchronous circuits with an example? 4.5 marks

3. a. Giving a neat diagram explain the structure of a fault simulator? 4.5 marks

b. Describe the Decision diagrams(BDT and BDD) of circuit(S1) for comparison the with its equivalent(S2) for formal verification. 4.5 marks

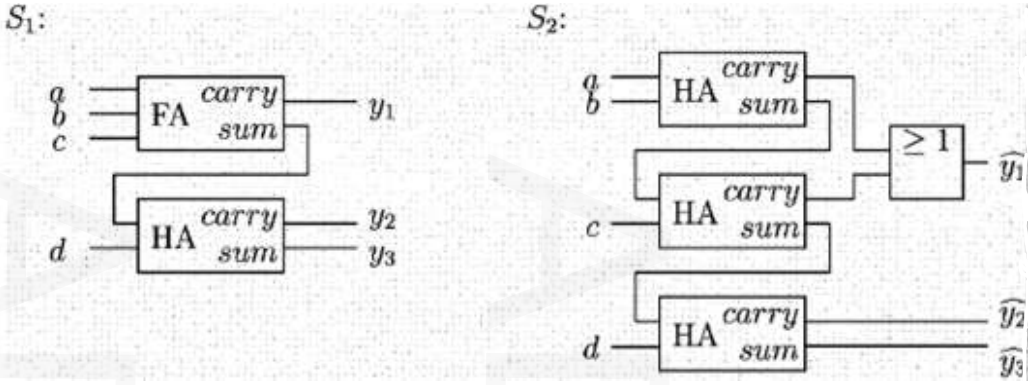

Fig1.

PART B

4. a. When is a fault detectable? Detect the fault s-a-0 in x4 in the following circuit? 4.5 marks

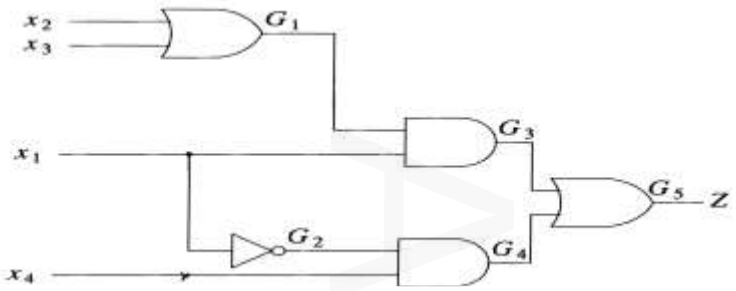

Fig2.

b. Discuss the different method of placement and routing for ASICs? 4.5 marks

5. a. With reference to the circuit given below explain sensitization for the fault marked in Fig3. 4.5 marks

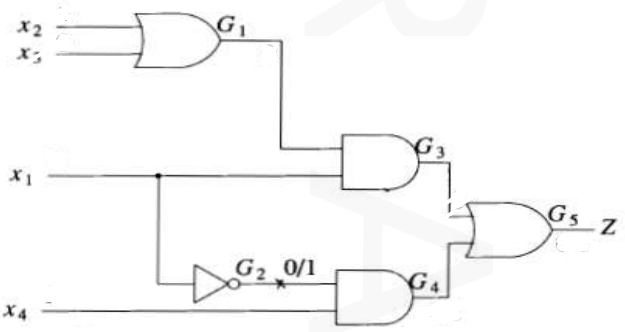

Fig3.

b. Explain the workflow for Geometric verification with a neat diagram? 4.5 marks

6. a. Discuss Serial Fault simulation with reference to the normal circuit given in Fig4. Assume s-a-0 at I2. Draw the scheduled event and activity list for the simulation. 4.5 marks

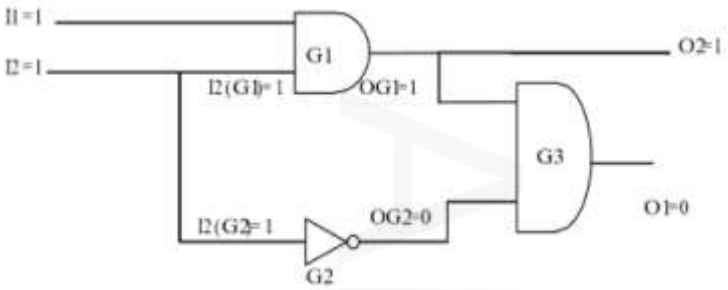

Fig4.

b.What are the different views of a library component according to Gajski chart? Discuss how standard cell libraries are designed? 4.5 marks

PART C

7. a. With diagrams explain the interfaces in Mixed signal simulation? What are the steps during the course of the simulation? 6 marks

b. Discuss the component geometries and different types of packages for professional PCB design EDA tools? 6 marks

8. a. Explain the mixed signal simulation for a NAND gate stating clearly the hierarchical representation? 6 marks

b. With a neat diagram explain the layout design flow for PCB? 6 marks

9. a. Discuss the SPICE concept? Briefly explain the different algorithms used for the simulations? 6 marks

b. Define Die Assembly in the context of IC processing? Discuss the main Die assembly methods? 6 marks