

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FIRST SEMESTER M.TECH DEGREE EXAMINATION

Electronics & Communication Engineering
(VLSI and Embedded Systems)

04EC6505—CMOS VLSI Design

Max. Marks : 60

Duration: 3 Hours

PART A

Answer All Questions

Each question carries 3 marks

1. Explain Tristate inverter with a neat circuit diagram?
2. Explain power dissipation in CMOS circuits?
3. Realize two input or gate with static CMOS logic? Explain the operation.
4. Explain CMOS D latch with a neat diagram?
5. Explain CMOS transmission gate implementation of the multiplexer?
6. Explain two input and gate with pass transistor logic?
7. Explain the problems associated with cascading of dynamic logic?
8. Implement ratio-less enhancement load dynamic shift register?

PART B

Each question carries 6 marks

9. Explain CMOS inverter circuit along with its VTC characteristics? Derive the expressions for V_{IL} , V_{IH} and V_{th} ?

OR

10. Design and explain the working of BICMOS inverter? What is latch up problem in CMOS circuits?
11. Explain logical effort of 4 input NAND and NOR gate?

OR

12. Explain about different delay models?
13. Realize the Boolean expression $Z = ABC + (D+E)F$ using static CMOS as well as using depletion type MOSFET as load?

OR

14. Realize XNOR function using full CMOS implementation method with 12 transistors?

15. Implement clocked NOR based SR latch circuit and JK latch circuit using depletion load MOSFET as load?

OR

16. Implement negative edge triggered master slave D flip-flop using CMOS logic?

17. Implement AND/NAND, OR/NOR and XOR/XNOR using Complimentary pass transistor logic?

OR

18. What are the advantages and disadvantages of pass transistor logic? Explain level restorer circuit in pass transistor logic?

19. Explain multiple output domino with an example?

OR

20. Explain true single phase clock dynamic CMOS logic? Explain the operation of TSPC based rising edge triggered D flip-flop?