Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Sixth semester B.Tech examinations (S), September 2020

Course Code: EC304

Course Name: VLSI

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks Marks

1 a) What is annealing? Explain the various types. (5)

b) Illustrate with diagram, the principle of crystal growth by Czochralzki method and Float zone process. Compare these processes. (10)

2 a) Determine the ratio of silicon consumed to the thickness of grown SiO_2 layer over silicon wafer. If SiO_2 layer of 0.4 μm is to be grown, what would be the thickness of used up silicon. Molecular weight of SiO_2 = 60.08g.mole, density of SiO_2 =2.2g/cm^3 , atomic weight of Si =20.09 g.mole, density of Si =2.33g/cm^3 (5)

b) Derive and explain Fick's 1st and 2nd laws (6)

c) What are the steps involved in photolithography process. (4)

3 a) Explain N-well CMOS IC fabrication sequence with neat diagrams. (9)

b) With the aid of neat diagrams explain fabrication process of transistors (6)

PART B

Answer any two full questions, each carries 15 marks

4 a) Implement the following functions using pass standard CMOS logic (6)
i) y = a AND b ii) y = a XNOR b

b) Draw the circuit diagram, stick diagram and layout of a CMOS inverter. (9)

5 a) Explain pass transistor logic. What are its demerits and how it can be remedied? (8)

b) Explain the DC output characteristics of CMOS inverter and discuss various regions in the characteristics. (7)

6 a) List the various types of power dissipation in CMOS. Which type is dominant and why? (5)

b) Explain the significance of design rules. What are the different design rules in CMOS technology? (5)

c) Discuss transmission gates. Implement XNOR gates using transmission gate logic. (5)

PART C

Answer any two full questions, each carries 20 marks

7	a)	Explain three different designs of ROM using CMOS transistors.	(10)
	b)	With neat figures and appropriate equations, explain the design of Linear Carry Select adders.	(10)
8	a)	With neat block diagram explain 4×4 bit-array multiplier.	(10)
	b)	Draw the CMOS implementation of a NAND ROM cell to store 4 words of 4bits each which are as follows 1010, 1000, 1101 and 1001.	(10)
9	a)	Explain six transistor CMOS SRAM cell .What are its merits and demerits.	(8)
	b)	Compare carry bypass adder and carry select adders.	(6)
	c)	With diagram, explain how a voltage sense amplifier can read and write a bit.	(6)

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