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**SLOT B**

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

FIRST SEMESTER M.TECH DEGREE EXAMINATION, APR 2021/DEC 2021

*Branch: Electronics & Communication*

*Stream: VLSI & Embedded Systems*

*Course Code & Name: 01EC6603 VLSI Technology & Design*

Answer *any two full* questions from *each* part

Limit answers to the required points.

Max. Marks: 60 Duration: 3 hours

**PART A**

1. a. Obtain the Drain characteristics & Transfer characteristics of n-channel Enhancement type MOSFET and explain its regions of operation. (4.5 marks)

   b. What is EGS? Explain the production of EGS from Hydrogen reduction of TrichloroSilane. (4.5 marks)

2. a. Explain the impact of Channel Length Modulation on Drain Current in Saturation region of a MOSFET. (4.5 marks)

   b. Give the principle involved in Molecular Beam Epitaxy. Explain MBE with a neat schematic of MBE Growth System. (4.5 marks)

3. a. What are Small Geometry Effects? Briefly explain the following Small Geometry Effects: (4.5 marks)

   i)Sub threshold Conduction & DIBL ii)Punch through

   b. Give short notes on Dry Etching & Wet Chemical Etching. Explain the significance of DC and AC Plasma excitation in etching Process. (4.5 marks)

**PART B**

4. a. Give the significance of the Physical Vapour Deposition methods in IC Processing. Explain Sputtering with a neat schematic diagram of sputtering system. (4.5 marks)

   b. Explain the functioning of Depletion-mode load NMOS Inverter. Obtain the inverter characteristics & specify its limitations. (4.5 marks)

5. a. Give the models of atomic diffusion mechanisms in solids. Derive Fick's 2nd law of diffusion. (4.5 marks)

   b. Explain the two methods by which dynamic power dissipation occurs in CMOS circuits. (4.5 marks)

6. a. Give the significance of below process in Ion Implantaion. (4.5 marks)
   i)Ion Stopping ii)Channeling

   b. What is pseudo NMOS logic? Implement the following: (4.5 marks)
      i) 4 input pseudo NMOS NOR gate
      ii) 4 input pseudo NMOS NAND gate

**PART C**

7. a. What is Bistability principle? Give the transistor level implementation of a CMOS clocked SR flip-flop and explain its working. (6 marks)

   b. Give short notes on the following: (6 marks)
   i)Fringing Capacitance ii)Skin Effect

8. a. With an example, explain how you will implement a monostable sequential circuit. (6 marks)

   b. Give the basic Rules in Stick diagram. Draw the Circuit diagram and its Stick diagram of 2 input Depletion mode NMOS NOR Gate. (6 marks)

9. a. Implement a 6 transistor CMOS SRAM cell. Explain its Read and Write operations. (6 marks)

   b. Give the significance of MOSFET scaling. Briefly explain Constant Field scaling used in MOSFET. (6 marks)