No.of pages:2 **A**

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FIRST SEMESTER M.TECH DEGREE EXAMINATION, APRIL 2021

VLSI and Embedded Systems
01EC6601 Digital System Design
Answer any two full questions from each part
Limit answers to the required points.

Max. Marks: 60 **Duration: 3 hours**

PART A

1)
a) Design the following function using PLA. Specify the PLA table.
(a) X = AB'D + A'C'+ BC + C'D'
(b) Y = A'C' + AC + C'D'
(c) Z = CD + A'C' + AB'D **4.5**
b) Design a Moore machine with output Z should be 1, if the input sequence ends in either 011 or 1001, and Z should be 0 otherwise. Implement with T flip flops. **4.5**

2)
a) Write a description on PAL 22V10. **4.5**
b) Distinguish between Mealy and Moore machine. **4.5**

3)
a) Design a sequential network to convert BCD to excess3 code. The input and output will be serial with the least significant bit first. **4.5**
b) How will you determine state equivalence using implication table? **4.5**

PART B

4)
a) How will you design a hazard free combinational network? **4.5**
b) Explain FPGA design flow. **4.5**

5)
a) How race free assignment is determined with the help of an adjacency diagram. **4.5**
b) Distinguish between SRAM based FPGA technology and anti- fuse based FPGA technology. **4.5**

6)

a) Distinguish between synchronous and asynchronous sequential circuits. **4.5**
b) Explain the routing structures available on an FPGA. **4.5**

PART C

7)

a) Construction of an SM chart for the control network of binary divider. **6**
b) Describe operator overloading and enumerated data types in VHDL with examples. **6**

8)

a) Explain different part of an SM chart. **6**
b) Explain procedure call in VHDL with example? Write down a function capable of converting integer to STD_LOGIC _VECTOR. **6**

9)

a) What is an SM chart? How will you convert state diagram to an SM chart. **6**
b) Differentiate various styles of modeling in VHDL. **6**