Reg No.:_____ Name:_____

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree (S,FE) Examination December 2020 (2015 Scheme)

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN (EC, AE)

Max. Marks: 100 Duration: 3 Hours

PART A

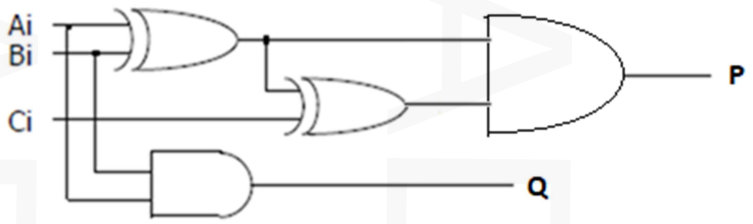
Answer any two full questions, each carries 15 marks. Marks

1 a) Convert the decimal number 963 to its equivalent Octal, Hexadecimal, BCD, Gray, XS-3 codes. (10)

b) Determine the Hamming code for the information 1101, with even parity. (5)

2 a) Simplify using K-map F(a,b,c,d) = ∑m (3,7,11,13,15)+ ∑d (0,12,14) and implement the circuit using NAND gates. (10)

b) Write expression for P and Q. (5)



3 a) Develop a full-subtractor circuit using a 3-to-8 decoder and gates. (9)

b) Consider two signed binary numbers A=0111 and B=1000 (B is in 2'complement form). Find A+B and A-B. Use 2's complement method for subtraction. Justify your answer. (6)

PART B

Answer any two full questions, each carries 15 marks.

4 a) Construct a 2 input NAND gate using CMOS. Explain its working with the help of truth table. (7)

b) Explain Fan-in, Fan-out, Propagation delay, and Noise margin of logic families. (8)

5 a) Design a mod-5 synchronous up counter using JK FF. (10)

b) Convert a D FF to T FF. (5)

6 a) Design a 3-bit ripple up counter using T FF and explain its working showing its timing diagram. (9)

b) Build a full adder circuit using PLA. (6)

PART C

Answer any two full questions, each carries 20 marks.

7 a) Construct a 4 bit serial-in serial-out ***left shift*** register using JK FF. Describe its operation on every clock pulse. (8)

b) Show the state table and Mealy model state diagram of JK FF. Derive its characteristic equation (12)

8 a) Design a 3-bit asynchronous up/down counter using JK FF that counts up when the mode M=1 and counts down when Mode=0. How does the circuit work (10)

b) Explain the working of a twisted ring counter, with the help of timing diagrams. (10)

9 a) Design a circuit to detect the sequence 1010 with overlapping, using D FF. Draw the state diagram, state table, excitation table and the circuit (10)

b) Minimize the state table using implication chart. (10)

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	d	b	0	0
b	e	a	0	1
c	g	f	0	1
d	a	d	1	0
e	a	d	1	0
f	c	b	0	0
g	a	e	1	0

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