

Reg No.: \_\_\_\_\_

Name: \_\_\_\_\_

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

Third Semester B.Tech Degree (S,FE) Examination December 2020 (2015 Scheme)

**Course Code: IT201****Course Name: DIGITAL SYSTEM DESIGN**

Max. Marks: 100

Duration: 3 Hours

**PART A***Answer any two full questions, each carries 15 marks.*

Marks

- 1 a) Convert  $(1657.8125)_{10}$  to binary and octal equivalents. (3)
- b) Subtract  $(482)_{10}$  from  $(136)_{10}$  using a) 1's complement method and b) 2's complement method. (6)
- c) Find the following.
- i)  $1010001.101 \times 1001.11$  (3)
- ii)  $100110100.0111 \div 1011.110$  (3)
- 2 a)  $(5A6BE)_{16} = (?)_8$  (2)
- b) Convert  $(FC1A7)_{16}$  to its binary equivalent and represent it in Single Precision floating point binary representation. (5)
- c) What is duality principle? Write down the basic theorems and postulates of Boolean Algebra. (8)
- 3 a) Prove that  $A + \overline{B}C(A + \overline{B}C) = A$  (2)
- b) Obtain the Canonical SOP expression for  $F = \overline{A}\overline{B}\overline{C} + \overline{B}C\overline{D} + \overline{A}BC\overline{D} + A\overline{B}\overline{C}$  and simplify it using K-map. (6)
- What are the limitations of simplification using K-map method?
- c) Simplify the Boolean function  $F(A,B,C,D) = \sum m(1,5,6,12,13,14) + d(2,4)$  using tabular method. (7)

**PART B***Answer any two full questions, each carries 15 marks.*

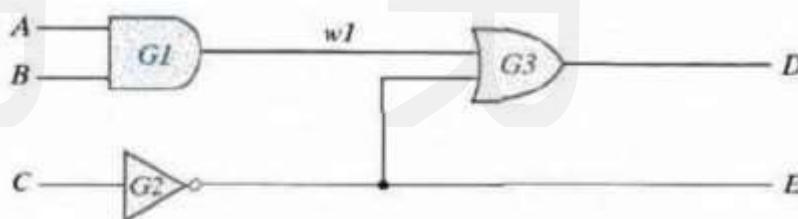
- 4 a) Design a Full Subtractor circuit and implement it using NAND gates only. (7)
- b) Design and explain Carry Look Ahead Adder. (8)
- 5 a) Design a 4-bit even parity bit generator. (4)

- b) Implement a full adder using two 4 x 1 MUX (5)
- c) Design a T flipflop from SR flipflop. (6)
- 6 a) What is an Excitation table? Give the excitation table of SR, JK, D and T flip flops. (5)
- b) Design the sequential circuit described by the following state equations. Use JK flip-flops. (10)
  - $A(t+1) = xAB + yA'C + xy$
  - $B(t+1) = xAC + y'BC'$
  - $C(t+1) = x'B + yAB'$

**PART C**

*Answer any two full questions, each carries 20 marks.*

- 7 a) Give the circuit diagram of Universal Shift Register. Explain its capabilities. (7)
- b) Design a Decade ripple counter using J-K Flipflop and explain it with the help of state diagram and timing diagram. (10)
- c) Discuss about the effect of propagation delay in clock period of ripple counters. (3)
- 8 a) Design a counter with binary count sequence 1-2-3-5-6-1. Use J-K flip flop to implement the counter. (6)
- b) Design a 4-bit Ring Counter using D flip flop. (4)
- c) Explain Hamming Code? Explain its error detection operation for the data word "11001010"? (10)
- 9 a) Draw and explain the logic diagram of a memory cell for storing one bit of information. (5)
- b) Give the hardware description of the circuit below in HDL (5)



- c) Draw the flow chart for signed magnitude multiplication algorithm. Explain with an example. (10)

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