Reg No.:__ Name:___

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree (S,FE) Examination December 2020 (2015 Scheme)

				Cor	urse Code	: EE2	203					
			Course Name	e: ANA	LOG ELI	ECTI	RONI	C CI	RCUI'	ΓS		
Max.	Ma	rks: 100								Dι	ıration: 3	8 Hours
					PART	A						
			Answei	r all qu	estions, ed	ich ce	arries	5 ma	rks.			Marks
1		With neat	circuit diagran	n, expla	ain the wor	king	of two	o leve	l clippe	er.		(5)
2		Explain	construction	and o	operation	of	deple	etion	type	metal	oxide	(5)
		semicondu	uctor FET with	neat d	iagram.							
3		An amplif	fier has a mid f	requen	cy gain of	100	and ba	andwi	dth of	200kHz	. What	(5)
		will be the	e new gain and	bandw	ridth if 5%	nega	tive fe	eedbac	ck is in	troduced	1?	
4		What are t	the characterist	ics of i	deal op-an	np? C	ompa	re it v	vith pra	actical o	pamp?	(5)
5		Explain th	ne working of z	ero cro	ssing detec	ctor.						(5)
6		Design an	adder circuit	to get	the outpu	t volt	tage a	ıs V _o	= - [2	V_1+3V_2	$+4V_{3}$],	(5)
		where V_1 ,	V_2 and V_3 are	inputs	to Op-Am	p.						
7		Draw and explain square wave generator using op –amp.							(5)			
8		Differentia	ate between a	stable	and mone	ostab	le mu	ıltivib	rator o	operation	n with	(5)
		waveform	ıs.									
					PART	В						
			Answer a	ny two	full quest	ions,	each	carrie	es 10 m	arks.		
9	a)	Derive the	e equation for	voltag	ge gain an	d cu	rrent	gain	for a I	BJT usi	ng h -	(6)
		parameter	model for Cor	nmon I	Emitter cor	ıfigur	ation.					
	b)	A CE am	plifier has the	h-para	meters giv	en by	y h _{ie} =	= 100	0Ω , h_{re}	e = 2.5	x 10 ⁻⁴ ,	(4)
		$h_{fe} = 50 a$	and $h_{oe} = 25 \text{ x}$	10 ⁻⁶ A/	V. If the 1	oad r	esistaı	nce R	L = 10	$\mathrm{k}\Omega$ and	source	
		resistance	is 100Ω , deter	rmine t	he (a) curr	ent ga	ain an	d (b)	voltage	gain.		
10	a)	In a potential divider biasing circuit, $V_{CC}=22V$, $R_1=39k\Omega$, $R_2=3.9k\Omega$,								(5)		
		$R_E = 1.5 k\Omega$, $R_C = 10 k\Omega$, β =100. Determine the operating point.										
	b)	Explain ho	ow FET can be	used a	s a voltage	cont	rolled	resis	tance.			(5)

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11		Draw and explain common source FET amplifier. Using small signal equivalent	(10)
		circuit, derive the expression for input impedance, output impedance and	
		voltage gain.	
		PART C	
12	a)	Answer any two full questions, each carries 10 marks. Draw the circuit diagram of a RC coupled amplifier. Explain the frequency	(5)
		response curve of RC coupled amplifier. Why does the gain fall off at low and	
		high frequencies?	
	b)	Prove that maximum efficiency of class B power amplifier is 78.5%.	(5)
13	a)	What is the role of coupling elements in multistage amplifiers? Compare	(6)
		different types of couplings used in multistage amplifier.	
	b)	Explain the following terms regarding an op-amp	(4)
		(i) CMRR, (ii) Slew rate	
14		With neat diagram, explain the working of Hartley oscillator. Derive the	(10)
		expression for frequency of oscillation.	
		PART D	
		Answer any two full questions, each carries 10 marks.	
15	a)	Explain how op-amp can be used as a differentiator.	(5)
	b)	Design a Schmitt trigger circuit with LTP= -5V and UTP= +5V. Explain its	(5)
		operation.	
16		With the help of internal functional diagram, explain the working of astable	(10)
		multivibrator using 555 timer.	
17	a)	Explain how logarithmic amplifier is realized using op-amp.	(5)
	b)	Design a Wein bridge oscillator using opamp to have an output frequency of 3.5kHz.	(5)
