02000CS203092001

Reg No.:_

Name:

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree (S,FE) Examination December 2020 (2015 Scheme)

Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN

Max	. Marks: 100 Durat	ion: 3 Hours
	PART A	
	Answer all questions, each carries 3 marks.	Marks
1	a) $(162)_8 + (537)_8 =$	(3)
	b) $(37A)_{16} + (4B9)_{16} =$	
2	Using truth table prove that (A+B)'= A'B'	(3)
3	Perform subtraction using 2's complement method.	(3)
	a) $(100)_2 - (110000)_2$	
	b) $(11010)_2 - (1101)_2$	
4	Express the given function in sum of minterms and product maxterms form.	(3)
	F(A,B,C) = C(A'+B) + B'C	
	PART B	
	Answer any two full questions, each carries 9 marks.	
5	a) Perform the following conversions.	(5)
	i) $(231B)_{16} = ()_2$	
	ii) $(574.32)_{10} = ()_2$	
	iii) $(10110011.01)_2 = ()_8$	
	iv) $(107)_8 = ()_{10}$	
	v) $(2671)_{10} = ()_{16}$	

- b) Convert the decimal number 5.62×10^3 to IEEE 754 standard single precision (4) floating point binary number.
- 6 a) Simplify the Boolean function F using the don't care conditions d, in SOP and (5) POS forms.

F(A,B,C,D)=A'B'D' + A'CD + A'BC

d(A,B,C,D) = A'BC'D + ACD + AB'D'

b) The sum of all minterms of a Boolean function of *n* variables is 1. (4)Prove the above statement for n=3.

02000CS203092001

7 a) Simplify the given function using Tabulation method and determine the prime (9) implicants, essential prime implicants and the minimized Boolean expression.
 F(A,B,C,D) = Σ(0,2,6,8,9,10,11,13,15)

PART C

Answer all questions, each carries 3 marks.

8	Implement Exclusive-OR using only NAND gates.	(3)
9	Draw the truth table and the logic circuit of a full adder.	(3)
10	Explain race around condition in JK flip-flop.	(3)
11	Draw the logic diagram of a D flip-flop using only NAND gates. Draw the	(3)
	characteristic table and obtain the characteristic equation.	

PART D

Answer any two full questions, each carries 9 marks.

12 a) A combinational circuit is defined by the following two functions. (5)

 $F_1 = x'y' + xyz'$

 $F_2 = x' + y$

Design the circuit with a decoder and external gates.

- b) Implement the function $F(A,B,C) = \Sigma(0,2,3,5)$ using a 2X1 MUX. (4)
- 13 a) Design a magnitude comparator that compares two 3 bit numbers A and B. (5)
 - b) Design a circuit that implements an SR flip-flop using a D flip-flop. (4)
- 14 a) A sequential circuit has two flip-flops A and B and one input x. The flip-flop (9) input functions are as follows.

 $J_A = xB$, $K_A = xB'$

 $J_B = x'A'$, $K_B = x + A$

Obtain the state table, state diagram and state equations.

PART E

Answer any four full questions, each carries 10 marks.

15	a)	Draw the circuit diagram of a 4-bit bidirectional shift register with parallel load	(10)
		and explain its working.	

- 16 a) Design a serial adder using a sequential-logic procedure (7)
 b) Explain the different types of ROMs. (3)
- 17 a) Design a counter with the following binary sequence: 0, 1, 3, 7, 6, 4 and repeat. (6) Use T flip-flops.
 - b) Write an HDL code for a half adder in structural style of modelling. (4)

02000CS203092001

18	a)	Explain PLA with a block diagram.	(4)
	b)	A combinational circuit is defined by the functions:	(6)
		$F_1(A,B,C) = \Sigma(3,5,6,7)$	
		$F_2(A,B,C) = \Sigma(0,2,4,7)$	
		Implement the circuit with a PLA having three inputs, four product terms and	
		two outputs.	
19	a)	Draw a flow chart and explain the addition and subtraction of two binary	(10)
		numbers in signed magnitude representation.	
20	a)	Differentiate between synchronous and asynchronous counters.	(4)
	b)	Draw the circuit diagram of a 4- bit binary ripple counter and explain its	(6)
		working.	

