Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fifth Semester B.Tech Degree Regular and Supplementary Examination December 2020

Course Code:EE365

Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 5 marks. Marks

1		What is Electronic design automation? What are its functions?	(5)
2		Explain about Generics in VHDL with examples.	(5)
3		What are the main components of an ASM chart? Explain.	(5)
4		Write the VDHL code for a D Flip Flop with output Q and Qbar.	(5)
5		What are the different constraints in RTL synthesis?	(5)
6		Explain the concept of event driven simulation.	(5)
7		Explain the necessity of testing digital systems.	(5)
8		Discuss fault oriented test pattern generation and overall strategy for generating test pattern.	(5)

PART B

Answer any two full questions, each carries 10 marks.

9	a)	Explain the basic electrical properties of CMOS circuits.	(5)
	b)	With the help of a neat block diagram explain how VHDL is used in the design process.	(5)
10	a)	Explain the implementation of NAND and NOR gate using CMOS Technology.	(5)
	b)	Write the VHDL code for a 2 to 4 Decoder.	(5)
11		Explain structural style of modelling in VHDL with suitable examples.	(10)

PART C

Answer any two full questions, each carries 10 marks.

12	a)	Design a state machine with two D Flip-Flops and one input X, when X=0 the state of the circuit remains the same, when X=1 the circuit goes through a transition from 00 to 01, then to 11 , then to 10 and back to 00. Draw the logical diagram, state diagram, state stable and ASM chart.	(10)

13	a)	Write and explain the VHDL code for an n bit binary up counter.	(5)
	b)	Write the VHDL model for SIPO right shift register.	(5)
14	a)	Explain the steps involved in design of a (synchronous sequential) digital system.	(5)
	b)	Explain how a ROM chip is modelled using VHDL.	(5)

PART D

Answer any two full questions, each carries 10 marks.

15		Explain simulation cycle of VHDL and its phases.	(10)
16		Explain the main component of IEEE .1149.1 boundary scan test architecture.	(10)
17	a)	Explain built in self-test scheme.	(5)
	b)	Explain compilation and elaboration process in VHDL.	(5)

****