

Reg No.: \_\_\_\_\_

Name: \_\_\_\_\_

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

Fifth Semester B.Tech Degree Regular and Supplementary Examination December 2020

**Course Code: EC361****Course Name: DIGITAL SYSTEM DESIGN**

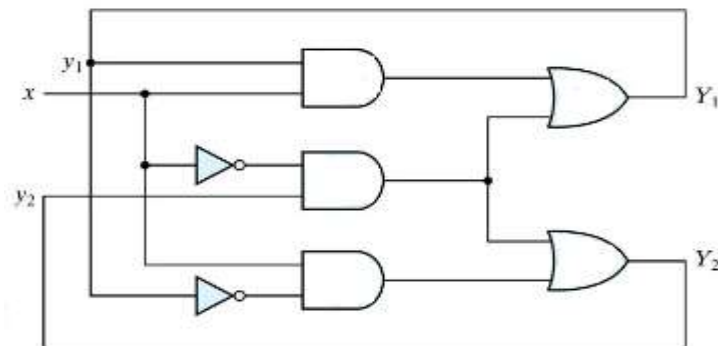
Max. Marks: 100

Duration: 3 Hours

**PART A***Answer any two full questions, each carries 15 marks.*

Marks

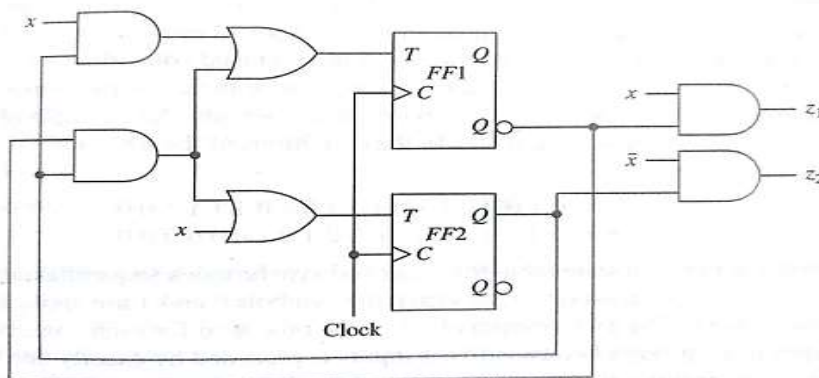
- 1 a) What are iterative circuits? Design an iterative circuit for a 4-bit ripple carry adder. (7)
- b) Design a CSSN using JK-FF having a single input line 'x' in which binary symbols 1 and 0 are applied. The network is to produce an output '1' with each 3<sup>rd</sup> multiple of 0 detected. All other times the output has to remain at '0'. Write the proper sample sequence before starting the design. (8)
- 2 a) Analyse the following fundamental mode asynchronous sequential circuit



(7)

- b) Design a coffee vending machine. The machine is to accept 5 and 10 rupees notes only. The amount for a coffee is 15 rupees. (It is not necessary that the machine gives the balance amount). (8)
- 3 a) Design a fundamental mode asynchronous sequential circuit meeting the following requirements:
- there are two inputs x and y, and single output z. (8)
  - x and y never change simultaneously.
  - the output is to be same as x if y = 1. However, if y = 0, the output should remain fixed at its last value before y became 0.

b) Analyse the below given CSSN.

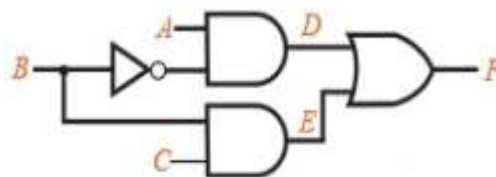


(7)

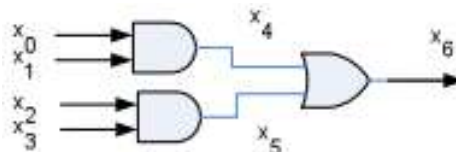
**PART B**

*Answer any two full questions, each carries 15 marks.*

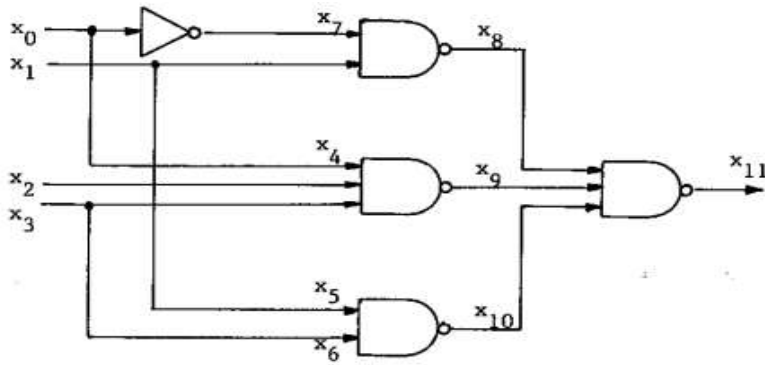
- 4 a) What do you mean by clock skew? Explain setup time, hold time, setup and hold violations with a neat timing diagram. How can we use clock skew to avoid the setup and hold violations? Justify. (8)
- b) Differentiate between static and dynamic hazards. What hazard exists in the circuit given below. Also derive the hazard free circuit. (7)



- 5 a) Find the minimal complete test for  $x_0, x_1, x_2$  and  $x_3, x_4$  and  $x_5$  for the below given circuit using the Fault table method. (8)



- b) What is a fault? How are faults classified? Define the terms: fault detection, fault location, test vector, Essential test vector, selective test vector and minimal complete test set. Explain the steps involved in the testing process. (7)
- 6 a) Using Path sensitisation method, find the test vectors for detecting SA0 and SA1 faults at  $x_7$  and  $x_9$ . (8)



- b) Explain essential hazards in asynchronous sequential networks with example. (7)  
 What are the constraints to be satisfied to avoid essential hazards?

**PART C**

*Answer any two full questions, each carries 20 marks.*

- 7 a) Explain different kinds of PLA folding. (10)  
 b) Describe the different test generation techniques for PLA. (10)
- 8 a) Examine the Input/output block of typical FPGA with the aid of a diagram. (10)  
 b) Describe the architecture of XC9500 CPLD with the help of a block diagram. (10)
- 9 a) Draw the simplified block diagram of Xilinx XC4000 configurable logic block (10)  
 and explain the various sections.  
 b) Write short notes on following: (10)  
 i) Design for testability ii) Built in self-test iii) PLA folding algorithm

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