Reg No.:_____   Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
Fifth Semester B.Tech Degree Regular and Supplementary Examination December 2020

Course Code: AE363
Course Name: VLSI CIRCUIT DESIGN

Max. Marks: 100   Duration: 3 Hours

PART A
Answer any two full questions, each carries 15 marks.   Marks

1 a) Explain drain induced barrier lowering and channel length modulation effects in MOSFET.   (8)

   b) With the help of neat diagram explain BICMOS technology.   (7)

2 a) With neat schematic explain the working of NMOS transistor and derive the current equation in linear and saturation region.   (8)

   b) Explain ion implantation in IC technology.   (7)

3 a) Describe accumulation, depletion and inversion region of formation in MOS device.   (7)

   b) Explain N-well CMOS IC fabrication with a neat sketch.   (8)

PART B
Answer any two full questions, each carries 15 marks.

4 a) Implement the logic function y=(AB+C(A+D))' using CMOS logic, obtain its stick diagram.   (8)

   b) Draw the stick diagram of two input NOR gate in CMOS logic.   (4)

   c) Implement XOR gate using domino logic.   (3)

5 a) Discuss the need for design rules. Explain lambda based design rules for CMOS.   (8)

   b) Explain NMOS inverter using depletion load.   (7)

6 a) Derive the pull up to pull down ratio for an NMOS inverter driven by another NMOS inverter.   (4)

   b) Draw the layout of 3 input NOR gate using NMOS logic.   (7)

   c) Explain pass transistor and transmission gates logic.   (4)

PART C
Answer any two full questions, each carries 20 marks.

7 a) Explain the latch based clocking.   (10)

b) Explain the clocked sequential circuit of JK and SR flipflop. (10)

8 a) Explain the scaling models and scaling factors for device parameters. (10)

b) Explain the dual rail coding used in signal generate completion signal. (10)

9 a) Explain the problem of skew and jitter. (10)

b) Explain arbiters. (10)

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