APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SEVENTH SEMESTER BTECH DEGREE (HONS.) EXAM DEC 19
Course code:04EC6209
Course Name: FPGA Based System Design

Max. Marks: 60 **Duration: 3 Hours**

Part A
Answer All Questions
Each question carries 3marks

1. Design a Half adder circuit using PAL.
2. What is meant by a CLB? Explain.
3. Draw the general architecture of Altera FPGA.
4. What is meant by a Lookup table . Give an example.
5. Give an example for Base Function..
6. List the various steps involved in design verification.
7. Explain general strategy of routing in FPGA.
8. Illustrate segmented routing..

Part B
Each question carries 6marks

9. With necessary diagrams explain MPGA.

OR

10. Differentiate SPLD and CPLD with reference to any two examples.

11. Explain static RAM Technology in detail.

OR

12. Explain any two applications of FPGA in detail.
13. With a neat diagram explain Xilinx design flow.

OR

14. Compare the performance of various commercially available FPGAs.
15. What is meant by logic synthesis. Explain

OR

16. Explain Chortle-crf technology mapper with necessary sketches.

17. Implement following functions using Xilinx XC 3000. How many CLBs and LUTs are required?

$$Y_1 = \overline{x} + y_1 \; ; Y_2 = x\,\overline{y_2} + \overline{x}\,\overline{y_1} \; ; \quad z = x \,.\, y_1$$

where Y_1, Y_2 are the next state variables and y_1, y_2 are the present state variables. Here **x** and **z** are inputs and outputs respectively.

OR

18. Explain multiplexer based technology mapping.

19. Explain K-segment routing for row based FPGA and discuss the results.

OR

20. What are the essential requirements for area effectiveness of FPGA? Explain?