Reg No.:_____   Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FOURTH SEMESTER B.TECH DEGREE EXAMINATION(S),DECEMBER 2019
Course Code: EE204
Course Name: DIGITAL ELECTRONICS AND LOGIC DESIGN

Max. Marks: 100   Duration: 3 Hours

PART A
Answer all questions, each carries 5 marks

Marks

1	a)	Convert $9B30_{16}$ to decimal .	5
	b)	Subtract $5C_{16}$ from 94_{16} .	
2		Convert Y=AB + B'CD into a product of max terms by algebraic method.	5
3		Design a full subtractor and show that it can be realized using two half subtractors.	5
4		Realize an S-R flip flop using D flip flop.	5
5		What is the importance preset and clear pin in flip flops? How they are utilised when designing a counter .	5
6		Explain Moore state machine model	5
7		Draw the schematic of a successive approximation A/D converter and explain working	5
8		Differentiate ROM, PLA and PAL circuits	5

PART B
Answer any two questions, each carries 10 marks

9	a)	Explain the gray code 10110010101 to binary numbers	3
	b)	Convert 1010.011_2 into decimal number	3
	c)	Add the hexadecimal numbers $DF_{16} + AC_{16}$	4
10	a)	Differentiate the methods of binary subtraction using 1's complement and 2's complement methods with suitable example.	5
	b)	Obtain the canonical product of sum form of the following function; F(A,B,C) = (A+B')(B+C)(A+C')	5
11	a)	Apply De-Morgan's theorems to the following expression (ABC)' + (D'+E)'	5
	b)	Using karnaugh map, simplify the expression $F(A,B,C,D) = \sum (0,2,3,5,7,8,13) + d(1,6,12)$	5

PART C
Answer any two questions, each carries 10 marks

12	a)	Design a full adder circuit with decoder I C	5

b) Realize a 4 bit parallel binary adder with look ahead carry generator   5

13 a) Implement the function $F(A,B,C,D) = \sum(0,1,3,4,8,9,15)$ using a suitable multiplier   5

b) What is the race around condition of a J-K flip flop? How can it be avoided   5

14 a) Show how a T flip flop can be converted to S-R flip flop   5

b) Draw a parallel in –serial out (PISO) register and explain its working   5

PART D
Answer any two questions, each carries 10 marks

15 a) Explain why Johnson counter have decoding gates,where as Ring counter does not?   5

b) Explain the design of a synchronous counter with modulus $< 2^n$,take MOD -5 counter as an example to illustrate   5

16 a) Construct a Johnson counter for 12 timing sequences.   5

b) Describe flash ADC and integrating type ADC   5

17 a) Design and implement a half adder and a full adder using VHDL   5

b) Explain FPGA and what are the advantages of FPGA over other types of PLD   5

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