Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SEVENTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

Course Code: CS405

Course Name: COMPUTER SYSTEM ARCHITECTURE

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks.

		Marks
1	A 400MHz processor was used to execute a program with 150000 floating point instructions with clock cycle count of 1. Determine the execution time and MIPS rate for this program.	(4)
2	State Amdahl's law. Write an expression for the overall speed up.	(4)
3	Distinguish between scalar RISC and super-scalar RISC in terms of instruction issue, pipeline architecture and performance.	(4)
4	Discuss the schematic representation of a generalized multiprocessor system.	(4)
5	Explain chained cache coherence protocol.	(4)
6	Consider the execution of a program of 15,00,000 instructions by a linear pipeline processor with a clock rate of 1000 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per cycle. The penalties due to branch instruction and out-of-order execution are ignored. a) Calculate the speedup factor in using this pipeline to execute the program as compared with the use of an equivalent non-pipelined processor with an equal amount of flow-through delay. b) Find out the efficiency and throughput of this pipelined processor.	(4)
7	Write short notes on internal data forwarding.	(4)
8	Explain Goodman's write once protocol with transition diagram.	(4)
9	List any two advantages and disadvantages of Scalable Coherence Interface(SCI).	(4)
10	What are the four context switching policies adopted by multithreaded architectures?	(4)

PART B

Answer any two full questions, each carries 9 marks.

11	a)	Discuss the Bernstein`s conditions for checking the parallelism among a set of processes.	(3)
	b)	Analyze the data dependences among the following statements and construct a	(6)

dependency graph. Also detect the parallelism embedded in them.

S1 : Load R1 , M(100) / R1 ← Memory(100) /
S2 : Move R2 , R1 / R2 ← (R1) /
S3 : Inc R1 / R1 ← (R1) + 1 /
S4 : Add R2 , R1 / R2 ← (R2) + (R1) /
S5 : Store M(100), R1 / Memory(100) ← (R1) /

12 a) Define the inclusion property of a memory hierarchy. Illustrate the data transfers between adjacent levels of a memory hierarchy. (5)

b) Consider a two-level memory hierarchy, M1 and M2 of sizes 64Kbytes and 4Mbytes respectively, with access time t1 = 20ns and t2 = 200ns and costs c1 and c2 are \$0.01/byte, c2 = \$0.0005/byte respectively. The cache hit ratio h1 = 0.95 at the first level. Find the effective access time and total cost of this memory system. (4)

13 Differentiate between the following with necessary diagrams:

a) UMA and NUMA multiprocessor models. (4)

b) RISC and CISC (5)

PART C

Answer any two full questions, each carries 9 marks.

14 a) Explain the different levels of hierarchy of bus systems. (4)

b) Define the write-invalidate snoopy bus protocol for maintaining cache coherence. Show the different possible state transitions for write-through and write-back cache using the write-invalidate protocol. (5)

15 Consider the five-stage pipelined processor specified by the following reservation table and answer the following: (S indicate the stages)

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X			
S4				X	X	

(i) List the set of forbidden latencies and the collision vector. (2)

(ii) Draw the state transition diagram showing all possible initial sequences without causing a collision in the pipeline. (3)

(iii) List all the simple and greedy cycles from the state diagram. (2)

(iv) Determine the minimal average latency (MAL). (2)

16 a) Explain the three major operational characteristics of a multiprocessor interconnection network. (3)

b) Analyse and compare the communication latencies of Store-and Forward and Wormhole routing schemes. (3)

c) Consider a 16-node hypercube network. Based on the E-cube routing algorithm, show how to route a message from node (0111) to node (1101). All intermediate nodes must be identified on the routing path. (3)

PART D

Answer any two full questions, each carries 12 marks.

17 a) Which are the three logic hazards possible in an instruction pipeline? Define each. Write the necessary conditions for each to occur. (6)

b) Explain the in-order and out-of-order pipeline scheduling policies for a superscalar machine with an example. (6)

18 a) Explain the importance of Tomasulo's algorithm for dynamic instruction scheduling. (8)

b) What do you mean by Release Consistency (RC) memory model? Give the conditions to ensure RC. (4)

19 a) Explain the effect of branching in instruction pipelining. Find the execution time and throughput of the pipeline for n instructions by considering the effect of branching. How branch penalty is reduced using delayed branch strategy. (6)

b) Explain any two latency hiding techniques used in distributed shared memory multi computers. (6)

****