

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FIFTH SEMESTER B. TECH DEGREE EXAMINATION(S), MAY 2019

Course Code: EC361

Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100

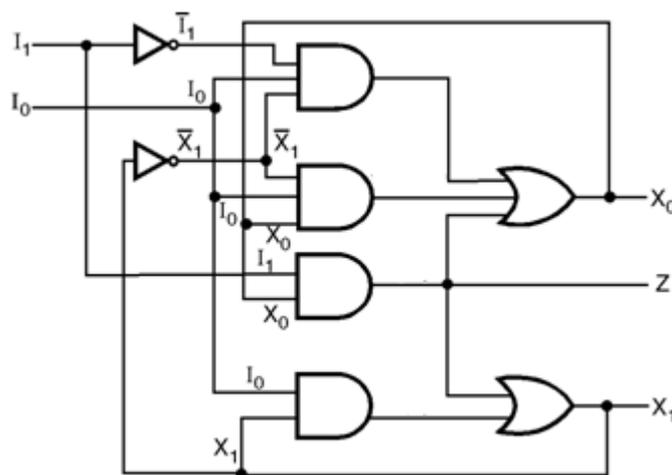
Duration: 3 Hours

PART A

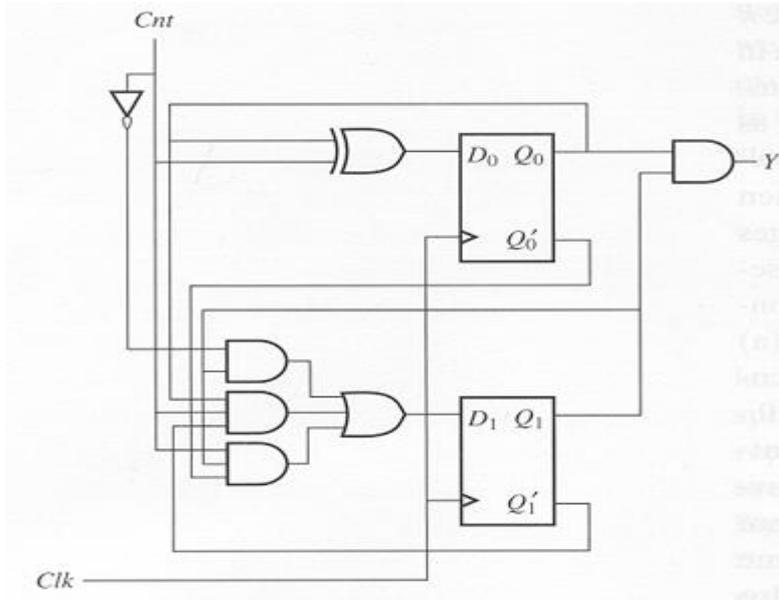
Answer any two full questions, each carries 15 marks.

Marks

- 1 a) Design a CSSN using T-FF having a single input line 'x' in which binary symbols 1 and 0 are applied. The network is to produce an output '1' coincident with the first 0 input symbol if it is preceded by exactly one or three 1 input symbols. All other times the output has to remain at 0. Write the proper sample sequence before starting the design. (8)
- b) Differentiate between state transition graph and ASM chart. Draw the ASM chart of a 3-bit up/down counter. How many ASM blocks are there in the ASM chart? (7)
- 2 a) There are two inputs x_1 and x_2 and single output z . The inputs x_1 and x_2 never change simultaneously. The output is to be 1 if x_1 was the last input variable to change value. On the hand, the output is to be 0 if x_2 was the last input variable to change value. Design a fundamental mode ASC based on the above behaviour. (8)
- b) Analyse the below given fundamental mode ASC (7)



- 3 a) Analyse the below given CSSN. (7)

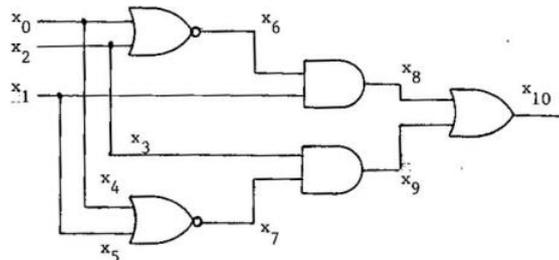


- b) Design a Pepsi vending machine. The machine is to accept 1 and 2 dollar notes (8)
only. The amount for a Pepsi is 5 dollars. (It is not necessary that the machine gives the balance amount).

PART B

Answer any two full questions, each carries 15 marks.

- 4 a) With neat circuit diagrams, differentiate between static and dynamic hazards. (for both 0 and 1 hazards in both) (7)
b) What do you mean by contact bounce? How do you eliminate contact bounce? (8)
Support the explanations with neat circuit diagrams and waveforms named clearly. Also draw the logic diagram for SR latch with the truth table.
- 5 a) Using path sensitization method, find the test vectors for detecting stuck at faults at \$x_6\$ and \$x_9\$ for the below given circuit. (8)



- b) Draw the logic diagram for the expression $f = a.b'.c + (d'.e')$. Find the test vectors (7)
for detecting the faults at input line a and d using Boolean difference method.

(Note: ' indicates complement).

- 6 a) Describe the Fault Table method used for effective test set generation for the circuit whose logic equation is $f = (a.b)' + b.d'$ (8)
- b) Explain different test pattern generation for BIST. (7)

PART C

Answer any two full questions, each carries 20 marks.

- 7 a) Implement the following functions using PLA and obtain their compatibility matrix. (10)
- $$f1(a,b,c,d) = \sum(1,2,3,4,5,6,8,10,13,15)$$
- $$f2(a,b,c,d) = \sum(2,9,10,12,14,15)$$
- b) Explain different kinds of PLA folding (10)
- 8 a) What are FPGAs? What are the differences between CPLD and FPGA? What are the advantages of FPGA? (8)
- b) Explain the architecture of XC 4000 FPGA family. (12)
- 9 a) Using suitable illustrations explain the XC4000 programmable interconnect. (10)
- b) Obtain the compatibility matrix for implementing the following functions: (10)
- $$z1(x1,x2,x3) = x1$$
- $$z2(x1,x2,x3) = x1.x2' + x1'.x2$$
- $$z3(x1,x2,x3) = x2'.x3 + x2.x3'$$
